



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,409	11/14/2001	Kazunori Sakurai	111109	7050

25944 7590 05/22/2003

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER

KILDAY, LISA A

ART UNIT PAPER NUMBER

2829

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/987,409

Applicant(s)

SAKURAI, KAZUNORI

Examiner

Lisa A Kilday

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 April 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) 8-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

Election/Restrictions

Applicant's election with traverse of method of manufacturing a semiconductor device in Paper No. 6 is acknowledged. The traversal is on the ground(s) that search is not burdensome. This is not found persuasive because for four reasons. First, the search is burdensome because at minimum it would cover classes 438, 257, 174, and 361 if the examiner examined claims 1-16. Second, it is recognized in the art that claims drawn to a device, circuit board, and electronic instrument are different. Third, the specification refers to the method, device, circuit board, and electronic instrument as different embodiments (pg. 2, lines 10 – pg. 8, line 6). Finally, the drawings of the inventions are different embodiments.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto (JP 2000-174044). Sakamoto discloses a method of manufacturing a semiconductor device comprising a step of mounting a semiconductor chip on a wiring substrate having a base substrate on which are formed interconnecting lines, wherein while melting the base substrate, bumps provided to the semiconductor chip are

Art Unit: 2829

pressed in, and the bumps are electrically connected to the interconnecting lines (abstract).

In re claim 2, Sakamoto discloses wherein the interconnecting lines comprise connecting portions electrically connecting with the bumps, and wherein in this step, the base substrate is melted, and the bumps and the connecting portions are sealed with the melted material of the base substrate (abstract).

In re claim 3, Sakamoto discloses wherein the melted material of the base substrate is adhered closely to a surface of the semiconductor chip (solution).

In re claim 4, Sakamoto discloses heating (¶8).

In re claim 5, Sakamoto discloses wherein a thermoplastic resin is used as the base substrate (solution).

In re claim 7, Sakamoto discloses a step of mounting another semiconductor chip on the wiring substrate (abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Imasu et al. (6,208,525). Sakamoto teaches a step of electrical connection that is at the same time of heating the semiconductor chip (abstract). However, Sakamoto does not teach a jig. However, Imasu et al. teaches in fig. 4b mounting a

Art Unit: 2829

semiconductor chip on a jig (30), heating the jig, electrically connecting the wiring (32b) and the bump electrodes (15), and pressing the semiconductor chip (10) on a substrate (col. 6, lines 21-41). Therefore, it would have been obvious at the time of the invention to modify the process of Sakamoto to include the steps of Imasu et al. because it is well known in the art to use a jig to heat a chip, electrically connect the chip, and press the chip on a substrate in order to make a bump electrode.

Conclusion


Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0957. See MPEP 203.08.

Any inquiry concerning this communication from the examiner should be directed to Lisa Kilday whose telephone number is (703) 306-5728. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo, can be reached on (703) 308-1233. The fax number for the group is (703) 305-3432. MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

Lisa Kilday

LAK

5/16/03


KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800